WHAT IS CLAIMED IS:

1. A ferroelectric memory device comprising:

an integrated circuit substrate;

a bottom interlayer dielectric layer on the integrated circuit substrate;

a plurality of ferroelectric capacitors arranged in a row and column relationship on the bottom interlayer dielectric layer;

a top interlayer dielectric layer disposed on a surface of the integrated circuit substrate including the plurality of ferroelectric capacitors, the top interlayer dielectric layer including via holes disposed on and associated with ones of the ferroelectric capacitors; and

a plate electrode formed in the top interlayer dielectric layer, the plate electrode extending into respective ones of the via holes to contact top surfaces of at least two neighboring ones of the plurality of ferroelectric capacitors.

2. The memory device of Claim 1, wherein the plate electrode comprises a local plate line and wherein the local plate line directly contacts the top surfaces of the ferroelectric capacitors arranged on at least two rows.

3. The memory device of Claim 2, further comprising a main plate line directly contacting a top surface of the local plate line through a slit type contact hole penetrating the top interlayer dielectric layer.

4. The memory device of Claim 1, wherein the plate electrode comprises:

a local plate electrode directly contacting the top surfaces of at least two neighboring ferroelectric capacitors; and

a main plate line directly contacting a top surface of a plurality of local plate electrodes arranged on at least one row through a silt type contact hole penetrating the top interlayer dielectric layer.

5. The memory device of Claim 1, wherein each of the ferroelectric capacitors is electrically connected to a predetermined region of the integrated circuit substrate through a storage node contact hole penetrating the bottom interlayer dielectric layer and wherein a diameter of the storage nod contact hole is greater at an

end thereof proximate an associated one of the ferroelectric capacitors than at an end thereof proximate the integrated circuit substrate.

6. The memory device of Claim 1, wherein the ferroelectric capacitors are stacked capacitors including a bottom electrode, a ferroelectric pattern and a top electrode and wherein the plate electrode directly contacts the top electrodes of ferroelectric capacitors arranged on at least two neighboring rows.

7. The memory device of Claim 1, further comprising a hydrogen barrier layer pattern interposed between the ferroelectric capacitors and the top interlayer dielectric layer, the via holes of the top interlayer dielectric layer extending through the hydrogen barrier layer to expose the top surfaces of the ferroelectric capacitors.

8. The memory device of Claim 7, wherein the hydrogen barrier layer extends along sidewalls of the ferroelectric capacitors and an edge portion of the top surfaces of the ferroelectric capacitors.

9. The memory device of Claim 1, further comprising a plurality of plate electrodes, each extending into respective ones of the via holes to contact top surfaces of at least two neighboring ones of the plurality of ferroelectric capacitors.

10. A ferroelectric memory device, comprising:

a plurality of cell transistors arranged in a row and column relationship on an integrated circuit substrate;

a bottom interlayer dielectric layer covering a surface of the integrated circuit substrate in a region including the plurality of cell transistors;

ferroelectric capacitors arranged in a row and column relationship on the bottom interlayer dielectric layer in the region including the plurality of cell transistors, the ferroelectric capacitors being electrically connected to associated ones of the cell transistors through respective storage node contact holes penetrating the bottom interlayer dielectric layer;

a top interlayer dielectric layer formed on the bottom interlayer dielectric layer including the ferroelectric capacitors, the top interlayer dielectric layer including a plurality of via holes disposed on the ferroelectric capacitors; and

a plurality of plate electrodes formed in the top interlayer dielectric layer and extending into respective ones of the via holes in the top interlayer dielectric layer to contact top surfaces of at least two neighboring ones of the ferroelectric capacitors.

11. The memory device of Claim 10, further comprising:

a slit type contact hole penetrating the top interlayer dielectric layer to expose plate electrodes arranged on at least one row; and

a main plate line covering the silt type contact hole.

12. The memory device of Claim 10, wherein the plate electrodes are local plate lines, each of which directly contacts the top surfaces of ferroelectric capacitors arranged on at least two rows.

13. The memory device of Claim 10, wherein the ferroelectric capacitors comprise stacked capacitors including a bottom electrode, a ferroelectric pattern and a top electrode and wherein each of the plate electrodes directly contacts at least two neighboring top electrodes.

14. A method of forming a ferroelectric memory device, the method comprising:

forming a bottom interlayer dielectric layer on an integrated circuit substrate;

forming a plurality of ferroelectric capacitors arranged in a row and column relationship on the bottom interlayer dielectric layer;

forming a top interlayer dielectric layer including via holes extending to the ferroelectric capacitors on the bottom interlayer dielectric layer and the plurality of ferroelectric capacitors; and

forming a plurality of plate electrodes on the top interlayer dielectric layer, each of the plate electrodes extending into ones of the via holes of the top interlayer dielectric layer to contact a top surface of at least two neighboring ferroelectric capacitors.

15. The method of Claim 14, wherein forming the plurality of ferroelectric capacitors includes:

forming a bottom electrode layer on the bottom interlayer dielectric layer;

forming a ferroelectric layer on the bottom electrode layer;

forming a top electrode layer on the ferroelectric layer; and

patterning the top electrode layer, the ferroelectric layer and the bottom electrode layer to form a plurality of stacked capacitors arranged in a row and column relationship on the bottom interlayer dielectric layer.

16. The method of Claim 14, wherein forming the top interlayer dielectric layer and forming the plate electrodes, comprises:

forming a first top interlayer dielectric layer on a region of the integrated circuit substrate including the ferroelectric capacitors;

patterning the first top interlayer dielectric layer to form a plurality of via holes exposing the top surfaces of the ferroelectric capacitors;

forming a bottom plate layer on the first top interlayer dielectric layer and extending into the plurality of via holes;

patterning the bottom plate layer to form a plurality of plate electrodes, each of which extends through ones of the via holes to contact the top surfaces of at least two neighboring ferroelectric capacitors; and

forming a second top interlayer dielectric layer on the first top interlayer dielectric layer and the plate electrodes.

17. The method of Claim 16, wherein each of the plate electrodes contacts the top surfaces of ferroelectric capacitors arranged on at least two neighboring rows.

18. The method of Claim 16, wherein forming the first top interlayer dielectric layer is preceded by forming a hydrogen barrier layer on the bottom interlayer dielectric layer and the plurality of ferroelectric capacitors and wherein forming the top interlayer dielectric layer includes forming the top interlayer dielectric layer on the hydrogen barrier layer including via holes extending through the hydrogen barrier layer to the ferroelectric capacitors.

19. The method of Claim 18, wherein the hydrogen barrier layer remains on sidewalls of the ferroelectric capacitors and an edge portion of the top surfaces of the ferroelectric capacitors after the via holes are formed in the top interlayer dielectric layer.

20. The method of Claim 16, further comprising:

patterning the second top interlayer dielectric layer to form a slit type contact hole parallel to a row that exposes plate electrodes on at least one row; and

forming a main plate line covering the slit type contact hole.